REMARKS

This is intended as a full and complete response to the Final Office Action dated October 16, 2008, having a shortened statutory period for response set to expire on January 16, 2009. Applicant submits this response to place the application in condition for allowance or in better form for appeal. Please reconsider the claims pending in the application for reasons discussed below.

Claims 1-12 are pending in the application. Claims 1-12 remain pending following entry of this response. Claims 1 and 5 have been amended. Applicant submits that the amendments do not introduce new matter.

Claim Rejections - 35 U.S.C. § 103

Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Dean et al.*, U.S. Patent No. 6,604,174 (hereinafter *Dean*) in view of *Hetherington et al.*, U.S. Publication No 2001/0010069 (hereinafter *Hetherington*).

The Examiner bears the initial burden of establishing a prima facie case of obviousness. See MPEP § 2141. Establishing a prima facie case of obviousness begins with first resolving the factual inquiries of Graham v. John Deere Co. 383 U.S. 1 (1966). The factual inquiries are as follows:

(A) determining the scope and content of the prior art;

(B) ascertaining the differences between the claimed invention and the prior art;

(C) resolving the level of ordinary skill in the art; and

(D) considering any objective indicia of nonobviousness.

Once the Graham factual inquiries are resolved, the Examiner must determine whether the claimed invention would have been obvious to one of ordinary skill in the art.

Respectfully, Applicant submits that the Examiner has not properly characterized the teachings of the references and/or the claims at issue. Accordingly, a prima facie case of obviousness has not been established.

For example, regarding claim 1 and the claims depending therefrom, the cited references do not disclose that a latency to access the allocated lines of the first private cache by the second processor is greater than a latency to access cache lines of a

second private cache associated with the second processor, wherein the first private cache and the second private cache are at a same cache level. Regarding accessing the first private cache and second private cache, Examiner cites paragraph [0007] of *Hetherington*, which is provided below.

> Modern processors support multiple cache levels, most often two or three levels of cache. A level 1 cache (L1 cache) is usually an internal cache built onto the same monolithic IC as the processor itself. On-chip cache is the fastest (i.e., lowest latency) because it is accessed by the internal components of the processor. On the other hand, off-chip cache is an external cache of static random access memory (SRAM) chips plugged into a motherboard. Off-chip cache has much higher latency, although is typically much shorter latency than accesses to main memory.

In other words, *Hetherington* simply states that the latency for accessing a cache in a first level (on chip cache) by a processor is smaller than the latency for accessing a cache in a second level (an off chip cache) by the same processor. Examiner seems to analogize the on chip cache and off chip cache of *Hetherington* with the first private cache and the second private cache respectively, as claimed. However, the on chip cache and the off chip cache of *Hetherington* are not at the same cache level. Accordingly, *Hetherington* does not disclose that a latency to access the allocated lines of the first private cache by the second processor is greater than a latency to access cache lines of a second private cache associated with the second processor, wherein the first private cache and the second private cache are at a same cache level.

For the same reasons stated above, regarding claim 5 and the claims depending therefrom, the cited references do not disclose that a latency to access the cache line of the second private cache by the first processor is greater than a latency to access cache lines of the first private cache associated with the first processor, wherein the first private cache and the second private cache are at a same cache level.

Therefore, the claims are believed to be allowable, and allowance of the claims is respectfully requested.

Conclusion

Having addressed all issues set out in the office action, Applicant respectfully submits that the claims are in condition for allowance and respectfully request that the claims be allowed.

If the Examiner believes any issues remain that prevent this application from going to issue, the Examiner is strongly encouraged to contact Gero McClellan, attorney of record, at (336) 698-4286, to discuss strategies for moving prosecution forward toward allowance.

Respectfully submitted, and
S-signed pursuant to 37 CFR 1.4,

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